Amendments of the Claims

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims

1. (previously presented) Receiver circuitry for adaptively equalizing a data signal, the receiver circuitry comprising:

equalization implementation circuitry that includes a selectable number of taps, wherein the equalization implementation circuitry operates on the data signal;

programmable circuitry that is programmed by configuration data with a first value corresponding to a first number of taps;

processing circuitry that computes a second value corresponding to a second number of taps; and

selection circuitry that selects, based on a control signal, one of the first and second values as the selectable number of taps at the time the programmable circuitry is being programmed by the configuration data, wherein the selection circuitry selects one of the first and second values only once while the equalization implementation circuitry operates on the data signal; and

wherein the selectable number of taps of the equalization implementation circuitry corresponds to the selected one of the first and second values.

2. (canceled)

3. (original) The circuitry defined in claim 1 wherein the processing circuitry performs an algorithm to compute the second number.

4. (previously presented) A digital processing system comprising:

processor circuitry;

a memory coupled to the processor circuitry; and

the receiver circuitry as defined in claim 1 coupled to the processor circuitry and the memory.

5. (previously presented) A printed circuit board on which is mounted receiver circuitry as defined in claim 1.

6. (previously presented) The printed circuit board defined in claim 5 further comprising:

a memory mounted on the printed circuit board and coupled to the receiver circuitry.

7. (previously presented) The printed circuit board defined in claim 5 further comprising:

processor circuitry mounted on the printed circuit board and coupled to the receiver circuitry.

8. (previously presented) Receiver circuitry for adaptively equalizing a data signal, the receiver circuitry comprising:

equalization implementation circuitry that includes a filter with taps having a selected one of integer tap spacing and fractional tap spacing relative to the symbol rate of the data signal, wherein the equalization implementation circuitry operates on the data signal;

programmable circuitry that is programmed by configuration data with a first value indicating a first selection between integer spacing and fractional spacing of the taps;

processing circuitry that computes a second value indicating a second selection between integer spacing and fractional spacing of the taps; and

selection circuitry that selects one of the first and second values as the selected one of integer spacing and fractional spacing at the time the programmable circuitry is being programmed by the configuration data, wherein the selection circuitry selects one of the first and second values only once while the equalization implementation circuitry operates on the data signal; and

wherein the selection between the integer and fractional tap spacing corresponds to the selected one of the first and second values.

9. (canceled)

10. (original) The circuitry defined in claim 8 wherein the processing circuitry performs an algorithm to compute the second selection.

11. (original) The circuitry defined in claim 8 wherein the fractional spacing is a selectable fraction of the symbol period, wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction.

12. (previously presented) Receiver circuitry for adaptively equalizing a data signal, the receiver circuitry comprising:

equalization implementation circuitry that includes at least one selectable coefficient value;

first processing circuitry for computing the coefficient value using a selectable starting value, wherein the coefficient value is different from the starting value;

programmable circuitry that is programmed by configuration data with a first starting value and outputs the first starting value and a control signal;

second processing circuitry that computes a second starting value and outputs the second starting value in parallel with the first value; and

selection circuitry that:

receives the control signal from the programmable circuitry, the first starting value and the second starting value in parallel;

selects, based on the control signal, one of the first and second starting values at the time the programmable

circuitry is being programmed by the configuration data, wherein the selection circuitry selects one of the first and second starting values only once; and

outputs the selected one of the first and second starting values to the first processing circuitry,

wherein the selectable starting value of the first processing circuitry corresponds to the selected one of the first and second values.

13. (canceled)

14. (original) The circuitry defined in claim 12 wherein the first processing circuitry performs an algorithm to compute the coefficient value.

15. (original) The circuitry defined in claim 12 wherein the second processing circuitry performs an algorithm to compute the second starting value.

16. (original) The circuitry defined in claim 12 further comprising:

further programmable circuitry for allowing selection between (1) operation of the first processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced.

17-19. (canceled)

20. (currently amended) The circuitry defined in claim 40 wherein the second processing circuitry performs an algorithm to compute the ~~first~~ second decision directed error signal.

21. (currently amended) The circuitry defined in claim 22 wherein the first processing circuitry performs an algorithm to compute the ~~second~~ first error signal using a training pattern.

22. (currently amended) Receiver circuitry for adaptively equalizing a received data signal, the receiver circuitry comprising:

first processing circuitry for computing [[an]] a first error signal using a selectable training pattern, wherein the first processing circuitry operates on the data signal;

programmable circuitry that is programmed by configuration data with a first training pattern and outputs the first training pattern and a first control signal;

training pattern circuitry that ~~computes~~ stores a second training pattern and outputs the second training pattern in parallel with the first training pattern; and

first selection circuitry that:

receives the first control signal from the programmable circuitry, the first training pattern and the second training pattern in parallel;

selects, based on the first control signal, one of the first and second training patterns at the time the programmable circuitry is being programmed by the configuration data, wherein the first selection circuitry selects one of the first and second training patterns only once while the processing circuitry operates on the data signal; and

outputs the selected one of the first and second training patterns to the first processing circuitry.

23. (canceled)

24. (previously presented) Receiver circuitry for adaptively equalizing a data signal, the receiver circuitry comprising:

equalization implementation circuitry, in the receiver circuitry, having at least one sampling point with a selectable location relative to a bit period of the received signal, wherein the equalization implementation circuitry operates on the data signal;

programmable circuitry that is programmed by configuration data with a first value corresponding to a first location of the sampling point and outputs the first value and a control signal;

processing circuitry that computes a second value corresponding to a second location of the sampling point and outputs the second value in parallel with the first value; and

selection circuitry that:

receives the control signal from the programmable circuitry, the first value and the second value in parallel;

selects, based on the control signal, one of the first and second values at the time the programmable circuitry is being programmed by the configuration data, wherein the selection circuitry selects one of the first and second values only once, while the equalization implementation circuitry operates on the data signal; and

outputs the selected one of the first and second values to the equalization implementation circuitry,

wherein the location of the at least one sampling point of the equalization implementation circuitry corresponds to the selected one of the first and second values.

25. (canceled)

26. (previously presented) A method of operating receiver circuitry having programmable circuitry and adaptive equalization capability, the method comprising:

programming the programmable circuitry using configuration data with a first value corresponding to a first number of taps;

computing a second value corresponding to a second number of taps;

selecting, at the time the programmable circuitry is being programmed by the configuration data, one of the first and second values, wherein the selecting selects one of the first and second values only once while equalization implementation circuitry operates on a data signal;

providing the selected one of the first and second values to the equalization implementation circuitry; and

controlling the equalization implementation circuitry to operate with a number of taps corresponding to the selected one of the first and second values.

27. (previously presented) A method of operating receiver circuitry having programmable circuitry and equalization implementation circuitry that includes a filter with taps, the method comprising:

programming the programmable circuitry using configuration data with a first value indicating a first selection between integer spacing and fractional spacing of the taps;

computing a second value indicating a second selection between integer spacing and fractional spacing of the taps;

selecting, at the time the programmable circuitry is being programmed by the configuration data, based on the received control signal, one of the received first and second values, wherein the selecting selects one of the received first

and second values only once while the equalization implementation circuitry operates on a data signal;

providing the selected one of the first and second values to the equalization implementation circuitry; and

controlling the filter of the equalization implementation circuitry, in the receiver circuitry, to operate with the tap spacing corresponding to the selected one of the first and second values.

28. (previously presented) A method of operating receiver circuitry having programmable circuitry and adaptive equalization capability, the method comprising:

programming the programmable circuitry using configuration data with a first starting value, wherein the programmable circuitry outputs the first starting value and a control signal;

computing a second starting value;

receiving the control signal, the first starting value and the second starting value in parallel;

selecting, at the time the programmable circuitry is being programmed by the configuration data, based on the received control signal, one of the received first and second starting values, wherein the selecting selects one of the received first and second values only once while equalization implementation circuitry operates on a data signal;

processing the selected one of the first and second starting values to compute a coefficient value different from the selected starting value; and

operating the equalization implementation circuitry, in the receiver circuitry, using the computed coefficient.

29. (canceled)

30. (currently amended) A method of operating receiver circuitry having programmable circuitry and adaptive equalization capability, the method comprising:

programming the programmable circuitry using configuration data with a first training pattern, wherein the programmable circuitry outputs the first training pattern and a first control ~~signals~~ signal;

computing a second training pattern to output the second training pattern;

receiving the first control signal, the first starting training pattern and the second training pattern in parallel; and

selecting, based on the first control signal, one of the received first and second training patterns at the time the programmable circuitry is being programmed by the configuration data, wherein the selecting selects one of the first and second the training patterns only once, based on the configuration data, while equalization implementation circuitry operates on a data signal.

31. (canceled)

32. (previously presented) A method of operating receiver circuitry having programmable circuitry and adaptive equalization capability, the method comprising:

programming the programmable circuitry using configuration data with a first value corresponding to a first sampling location, wherein the programmable circuitry outputs the first value and a control signal;

computing a second value corresponding to a second sampling location;

receiving the control signal, the first value and the second value in parallel;

selecting, at the time the programmable circuitry is being programmed by the configuration data, based on the received control signal, one of the received first and second values, wherein the selecting selects one of the received first and second values only once only once while equalization implementation circuitry operates on the data signal;

providing the selected one of the first and second values to the equalization implementation circuitry; and

operating the equalization implementation circuitry, in the receiver circuitry, using the sampling location corresponding to the selected one of the first and second values.

33. (previously presented) The circuitry defined in claim 1 wherein the programmable circuitry comprises first and second programmable elements, wherein the first programmable element allows the first value to be specified and the second

programmable element controls the selection made by the selection circuitry.

34. (previously presented) The circuitry defined in claim 8 wherein the programmable circuitry comprises first and second programmable elements, wherein the first programmable element allows the first value to be specified and the second programmable element controls the selection made by the selection circuitry.

35. (previously presented) The circuitry defined in claim 12 wherein the programmable circuitry comprises first and second programmable elements, wherein the first programmable element allows the first starting value to be specified and the second programmable element provides the first control signal.

36. (previously presented) The circuitry defined in claim 22 wherein the programmable circuitry comprises first and second programmable elements, wherein the first programmable element allows the first training pattern to be specified and the second programmable element provides the first control signal.

37. (previously presented) The circuitry defined in claim 24 wherein the programmable circuitry comprises first and second programmable elements, wherein the first programmable element allows the value to be specified and the second programmable element provides the control signal.

38. (previously presented) The circuitry defined in claim 1 wherein:

the programmable circuitry outputs the first value and a control signal;

the processing circuitry outputs the second value in parallel with the first value;

the selection circuitry:

receives the control signal from the programmable circuitry, the first value and the second value in parallel;

selects, based on the received control signal, one of the first and second values; and

outputs the selected one of the first and second values to the equalization implementation circuitry.

39. (previously presented) The circuitry defined in claim 8 wherein:

the programmable circuitry outputs the first value and a control signal;

the processing circuitry outputs the second value in parallel with the first value; and

the selection circuitry:

receives the control signal from the programmable circuitry, the first value and the second value in parallel;

selects, based on the control signal, one of the first and second values; and

outputs the selected one of the first and second values to the equalization implementation circuitry.

40. (currently amended) The circuitry defined in claim 22 further comprising:

equalization implementation circuitry responsive to an error signal, wherein the equalization implementation circuitry operates on the data signal;

wherein the first processing circuitry receives the selected one of the first and second training patterns and computes [[a]] the first error signal using the selected training pattern and outputs the first error signal;

second processing circuitry that computes a second decision directed error signal using a training pattern and outputs the second error signal in parallel with the first error signal; and

second selection circuitry that:

receives a second control signal from the programmable circuitry, the first error signal and the second error signal in parallel;

selects, based on the second control signal, one of the first and second error signals; and

outputs the selected one of the first and second error signals to the equalization implementation circuitry,

wherein the equalization implementation circuitry is responsive to the selected one of the first and second error signals.

41. (previously presented) The method of claim 26 wherein:

the programmable circuitry outputs the first value and a control signal; and

the control signal, the first value and the second value are received in parallel.

42. (previously presented) The method of claim 27 wherein:

the programmable circuitry outputs the first value and a control signal; and

the control signal, the first value and the second value are received in parallel.

43. (previously presented) The method of claim 28 further comprising:

selecting, at the time the programmable circuitry is being programmed by the configuration data, whether the computed coefficient to be used in equalization implementation circuitry is to be determined once or on an on-going basis; and

determining the computed coefficient in accordance with the selecting.

44. (previously presented) The method of claim 30 further comprising:

computing a first error signal based on the selected training pattern;

computing a second decision directed error signal based on a training pattern;

receiving the second control signal, the first error signal and the second error signal in parallel;

selecting, based on a second control signal provided by the programmable circuitry, one of the received first and second error signals; and

using the selected one of the first and second error signals in a determination of at least one operating parameter of the equalization implementation circuitry.